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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/433,677	11/04/1999	SYWE N. LEE	6762-102XX	2847

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EXAMINER
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MOE, AUNG SOE

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
09/433,677

Applicant(s)  
LEE et al.

Examiner  
Aung Moe

Art Unit  
2612



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Jun 29, 2001
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2 6) ☐ Other:

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## DETAILED ACTION

### *Specification*

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to **a single paragraph** on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the abstract should be limited to a single paragraph. Correction is required. See MPEP § 608.01(b).

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***Drawings***

3. Figures 1A and 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Objections***

4. Claims 1-6 and 7 are objected to because of the following informalities:

In claim 1, lines 23, please change "analog signals" to -- said analog signals -- because "analog signals" were previously recited in lines 4 of claim 1.

In claim 7, line 14, please change the word "phododiodes" to -- photodiodes--.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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6. Claims 1 and 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunaga et al. (U.S. 6,091,449).

Regarding claim 1, Matsunaga '449 discloses an image sensor for sensing the light of an image impinging thereupon and for translating the image into a standard television format (i.e., col. 1, lines 15+ and col. 4, lines 35-45), said image sensor comprising a plurality of pairs of light-detecting elements (i.e., Figs. 7, 30 and 33; the elements' P1-1-1, . . . ) arranged in rows and columns for generating respective analog signals in proportion to the intensity of the light impinging respectively one one of the light-detecting elements (i.e., the elements' 62a/62b), characterized in that each pair of light-detecting elements comprises:

a first photodiode (i.e., the element's 62a); a second photodiode (i.e., the element's 62b); at least one turn-on transistor (i.e., the transistor 63a/b) coupled to each of said first and second photodiodes (i.e., the elements' 62a/b) and having a gate (i.e., col. 8, lines 45+), wherein said first and second photodiodes (i.e., the elements' 62a/b) in each pair of light-detecting elements (i.e., the elements' P1-1-1, . . . ) Are coupled in parallel in the column direction at a floating sensing point through said at least one trun-on transistor (i.e., see Figs. 7, 30 and 33; col. 8, lines 40+, col. 9, lines 15+ and col. 21, lines 10+ and col. 22, lines 16+); and

translating means (i.e., Figs. 7, 30 and 33; col. 8, lines 40+, col. 9, lines 15+ and col. 21, lines 10+ and col. 22, lines 16+) coupled to said floating sensing point for resetting the initial state of said floating sensing point and reading out said analog signals to a column line (8-1, . . . , 8-n); wherein said first and second photodiodes (i.e., 62a/b) in adjacent pairs of light detecting

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elements (P1-1-1, . . . ) are coupled in parallel in the column direction such that said at least one turn-on transistors (i.e., 63a/b) coupled to said first and second photodiodes (i.e., 62a/b) are sequentially controlled by first and second gate control lines (i.e., noted the lines 22-1 and 24-1) coupled to the gate of said at lest one turn-on transistor (i.e., the elements' 63a/b), respectively and the analog signals acquired in said first and second photodiodes (i.e., the elements' 62a/b) of one of the same pairs and the adjacent pair present at said floating sensing point in response to one of said first and second gate control lines (i.e., the lines 22-1/24-1), thereby enhancing the light sensitivity of said image sensor (i.e., see col. 1, lines 14+, col. 8, lines 40+, col. 9, lines 15+ and col. 21, lines 10+ and col. 22, lines 16+).

Regarding claim 3, Matsunaga '449 discloses wherein said translating means (i.e., Figs. 7, 30 and 33, the element's 68) further comprises an amplifier transistor for amplifying the analog signals presenting at said floating sensing point (i.e., col. 8, lines 53+).

Regarding claim 4, Matsunaga '449 discloses wherein said translating means comprises a reset transistor for resetting the initial state of said floating sensing point in response to a reset signal (i.e., col. 8, lines 65+) and a source follower transistor and another turn-on transistor coupled to said column line (i.e., Figs. 3, 7, 21, 30 and 33; col. 8, lines 8-68).

Regarding claim 5, Matsunaga '449 discloses wherein said first and second photodiodes (i.e., 62a/62b) in each pair of light-detecting elements (i.e., a unit cell P1-1-1) each connects to one turn-on transistor enable by a specific gate control line such that said first and second photodiodes are coupled together at said floating sensing point in response to said specific gate

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control lines (i.e., see Figs. 3, 7-8, 26, 30-33; col. 8, lines 35-col. 9, lines 68 and col. 10, lines 15+).

Regarding claim 6, Matsunaga '449 discloses wherein said first and second photodiodes (62a/62b) in each pairs of light-detecting elements (i.e., a unit cell P1-1-1) each connects to two turn-on transistors (i.e., 63a/63b) enabled by two different gate control lines (i.e., 22-1/24-1) such that said first and second photodiodes (62a/62b) are coupled together at said floating sensing point (i.e., see Figs. 7, 30 and 33).

Regarding claim 7, Matsunaga '449 discloses a method for use in an image sensor for sensing the light of an image impinging thereupon and for translating the image into a selected television format comprising a plurality of pairs of light-detecting elements arranged in rows and columns for generating respective analog signals in proportion to the intensity of the light impinging respectively on one of the light-detecting elements (i.e., see Figs. 3, 7, 30 and 33, the cell units' P1-1-1) comprising:

a first photodiode (i.e., 62a); a second photodiode (62b), at least one turn-on transistor coupled to each of said first and second photodiodes (62a/62b) and having a gate, wherein said first and second photodiodes in each pair of light-detecting elements are coupled in parallel in the column direction at a floating sensing point through said at least one turn-on transistor and translating means coupled to said floating sensing point for resetting the initial state of said floating sensing point and reading out said analog signals to a column line (i.e., the element 8-1), wherein said first and second photodiodes (62a/62b) in adjacent pairs of light-detecting elements

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are coupled in parallel in the column direction (Figs. 7, 30 and 33; col. 9, lines 15+), the method comprising the steps of:

generating respective analog signals in proportion to the intensity of the light impinging on respective one of the light-detecting elements (i.e., col. 10, lines 15+);

sequentially enabling the gates of said first gate control lines (i.e., the lines 22-1; col. 10, lines 20+) and then the gates of said second gate control lines (i.e., Figs. 8, 20, 23; col. 10, lines 45+); and

obtaining said analog signals acquired in said first and second photodiodes of one of the same pairs and the adjacent pairs presented at said floating sensing point, in response to one of said first and second gate control lines (i.e., Figs. 7, 30 and 33; col. 8, lines 80+; col. 10, lines 10+).

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.



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This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim ~~1~~<sup>2</sup> is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga '449 in view of Elabd (U.S. 5,272,535).

Regarding claim ~~1~~<sup>2</sup>, Matsunaga '449 discloses wherein said analog signals acquired in said photodiodes (62a/62b) controlled by said first gate control lines (22-1) constitute first field signals (i.e., col. 4, lines 35-45 and col. 11, lines 5+) and said analog signals acquired in said photodiodes (62a/62b) controlled by said second gate control lines (24-1) constitute second field signals (i.e., noted the frame interval read out as shown in Figs. 8, 23, 28; see col. 11, lines 5+), wherein the components of said first field and second signals are correlated with one another (i.e., as shown in Fig. 3, the signals read out for one frame interval includes a first and second fields' intervals correlated with one another), thereby improving the quality of the television image signals (i.e., col. 4, lines 40+, col. 1, lines 5+ and col. 22, lines 60+).

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Furthermore, it noted that Matsunaga '449 does not explicitly state that the time difference of the first and second fields signal is less than  $1/60$  second as recited in present claimed invention.

However, the above mentioned claimed limitations are well-known in the art as evidenced by Elabd '535. In particular, Elabd '535 teaches that in order to improve the quality of the image displayed in a television (i.e., removing edge distortion interline flicker and field-to-field flicker noise of interlacing video signals; see col. 6, lines 55+), it is obviously well-known in the art to implement the time difference of the first and second field signals which is less than  $1/60$  second so that it would improve the quality of the image displayed (i.e., Noted the use of a display device as shown in Fig. 1A of Elabd '535) in a television as recited in the present claimed invention (i.e., see col. 7, lines 50-68).

In view of the above, having the system of Matsunaga '449 and then given the well-established teaching of Elabd '535, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsunaga '449 as taught by Elabd '535, since Elabd '535 states at column 6, lines 55+ that such a modification would remove edge distortion interline flicker and field-to-field flicker noise thereof.

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***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Hamasaki '459, Chow '365, Hosier '013, Shigenaka '860, Hairston '570 and Wyles '005 show an image sensor for sensing the light of an image impinging thereupon and the image sensor comprising a plurality of pairs of light-detecting elements arranged in rows and columns for generating respective analog signals in proportion in the intensity of the light impinging respectively on one of the light-detecting elements; and wherein the first and second photodiodes are coupled in parallel direction.

b. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Aung S. Moe** whose telephone number is (703) 306-3021. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wendy Garber**, can be reach on (703) 305-4929.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

**or faxed to:**

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**(703) 872-9314**, (for informal or draft communications, please label  
"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,  
Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to  
the customer service number **(703) 306-0377**.

A. Moe

June 27, 2003

  
**AUNG S. MOE**  
**PATENT EXAMINER**